

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of the claims in the application.

Listing of Claims:

1 1. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device having a plurality
3 of first MISFETs in a first region of a semiconductor
4 substrate and a plurality of second MISFETs in a second
5 region of said semiconductor substrate, comprising the
6 steps of:

7 (a) forming a plurality of first insulating film
8 portions in each of ~~between two adjacent regions of said~~
9 first MISFET forming regions in said first region and said
10 second MISFET forming regions in said second region,

11 (b) forming a plurality of second insulating film
12 portions over a surface of said semiconductor substrate
13 ~~between said first insulating films~~ film portions in each of
14 said first and second regions,

15 (c) depositing ~~[[a]]~~ third insulating film portions
16 over at least said second insulating film portions and said
17 first insulating film portions,

18 (d) forming [[a]] first conductive film portions over
19 said third insulating film portions in said second region,
20 (e) forming, after removal of portions of said third
21 and second insulating films from said first region, [[a]]
22 fourth insulating film portions over the surface of said
23 semiconductor substrate in said first region, [[and]]
24 (f) forming [[a]] second conductive film portions over
25 said fourth insulating film portions,
26 (g) forming a fifth insulating film covering said
27 semiconductor substrate, and
28 (h) forming a plurality of first interconnects over
29 said fifth insulating film
30 ~~(g) wherein said third insulating film remains over~~
31 ~~said first insulating film in said second region.~~

1 2. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 1, wherein each said first insulating film portion is an
4 oxide film formed by thermal oxidation.

1 3. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 1, wherein said third insulating film [[is]] portions are

4 formed by CVD.

1 4. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 1, wherein an etching rate of said third insulating film
4 portions is greater than that of said first insulating film
5 portions.

1 5. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 1, wherein said third insulating film ~~[[is]]~~ portions are
4 thicker than said second insulating film portions.

1 6. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 1, wherein said first and second conductive ~~films~~ film
4 portions are each made of polysilicon.

1 7. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 1, wherein ~~[[the]]~~ a third insulating film portion over
4 said a first insulating film portion is formed so that end
5 portions of said third insulating film ~~is~~ portion are

6 positioned on said first insulating film portion.

1 8. (Withdrawn) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 1, wherein said first insulating film forming step
4 comprises forming a groove in said semiconductor substrate
5 and forming an oxide film within said groove.

1 9. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 1, wherein the first insulating film portions in said first
4 region ~~[[is]]~~are narrower than the first insulating film
5 portions in said second region.

1 10. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 1, wherein said a first insulating film portion in said
4 second region is also formed at ~~both~~with parts underlying
5 ends of said a first conductive film portion~~forming region~~.

1 11. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 1, wherein said first insulating film ~~is also~~ portions

4 include portions formed at both ends of the first
5 ~~conductive film~~ second MISFET forming region regions within
6 said second region, and

7 said manufacturing method further comprises forming
8 first semiconductor regions in the semiconductor substrate
9 below the first insulating film formed portions at both
10 ends of said ~~first conductive film~~ second MISFET forming
11 region regions, and

12 forming second semiconductor regions within said first
13 semiconductor regions but ~~outside of~~ beside the first
14 insulating film formed portions at both the ends of the
15 ~~first conductive film~~ said second MISFET forming region
16 regions.

1 12. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 ~~[[1]]~~ 11, wherein the impurity concentration of said first
4 semiconductor regions is lower than that of said second
5 semiconductor regions.

1 13. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device having a plurality
3 of first MISFETs in a first region of a semiconductor

4 substrate and a plurality of second MISFETs in a second
5 region of said semiconductor substrate, comprising the
6 steps of:

7 (a) forming a plurality of first insulating film
8 portions in each of between two adjacent regions of said
9 first MISFET forming regions in said first region and said
10 second MISFET forming regions in said second region,

11 (b) forming a plurality of second insulating film on
12 portions over a surface of the semiconductor substrate
13 between said first insulating films film portions in said
14 first and second regions,

15 (c) depositing [[a]] third insulating film portions
16 over at least said second insulating film portions and said
17 first insulating film portions,

18 (d) removing said third insulating film portions from
19 said first region without removing said third insulating
20 film over said first insulating film portions in said
21 second region,

22 (e) depositing a first conductive film in said first
23 and second regions on over said semiconductor substrate,

24 (f) removing said first conductive film from said
25 first region and a portion of said first conductive film
26 from said second region,

27 (g) forming [[a]] fourth insulating film on portions
28 over the surface of said semiconductor substrate in said
29 first region, [[and]]

30 (h) forming a second conductive film in said first
31 region,

32 (i) forming a fifth insulating film over at least said
33 first and second MISFET forming regions and said third
34 insulating film portions formed over said first insulating
35 film portions, and

36 (j) forming a plurality of first interconnects over
37 said fifth insulating film.

1 14. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 13, wherein each said first insulating film is an oxide
4 film formed by thermal oxidation.

1 15. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 13, wherein said third insulating film [[is]] portions are
4 formed by CVD.

1 16. (Currently amended) A manufacturing method of a

2 semiconductor integrated circuit device according to claim
3 13, wherein an etching rate of said third insulating film
4 portions is greater than that of said first insulating film
5 portions.

1 17. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 13, further comprising, between said step (d) and said step
4 (e), heat treating said third insulating film portions.

1 18. (original) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 17, wherein said heat treatment is conducted at 900°C or
4 greater.

1 19. (original) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 17, wherein said heat treatment is conducted at 1000°C or
4 greater.

1 20. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 13, wherein said third insulating film [[is]] portions are

4 thicker than said second insulating film portions.

1 21. (original) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 13, wherein said first and second conductive films are each
4 made of polysilicon.

1 22. (withdrawn) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 13, wherein said first insulating film forming step
4 comprises forming a groove in said semiconductor substrate
5 and forming an oxide film in said groove.

1 23. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 13, wherein the first insulating film portions in said
4 first region [[is]] are narrower than the first insulating
5 film portions in said second region.

1 24. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device having, in a first
3 region of a semiconductor substrate, a plurality of first
4 MISFETs each equipped with a gate electrode and source

5 drain regions and, in a second region of said semiconductor
6 substrate, a plurality of second MISFETs each equipped with
7 a gate electrode and source drain regions, comprising the
8 steps of:

9 (a) forming a plurality of first insulating film
10 portions in each of between two adjacent regions of said
11 first MISFET forming regions in said first region and said
12 second MISFET forming regions in said second region,

13 (b) introducing impurities in said second region,
14 thereby forming a first semiconductor region in said first
15 region and a second first semiconductor region regions as
16 portions of the source and drain regions of said second
17 MISFETs in said second region,

18 (c) forming a plurality of second insulating film on
19 portions over a surface of said semiconductor substrate
20 between said first insulating films film portions,

21 (d) depositing [[a]] third insulating film portions
22 over at least said second insulating film portions and said
23 first insulating film portions,

24 (e) removing said second and third insulating films
25 film portions in said first region, and removing a portion
26 of the said second and third insulating films film portions
27 over a said second first semiconductor region in said

28 ~~second region, thereby forming a first opening,~~

29 (f) forming [[a]] first conductive film portions to be
30 a provide gate electrode electrodes of said second MISFET
31 MISFETs over said third insulating film portions between
32 said first insulating film portions in said second region
33 ~~of said semiconductor substrate,~~

34 (g) forming [[a]] fourth insulating film portions over
35 the surface of the semiconductor substrate in said first
36 region,

37 (h) forming [[a]] second conductive film portions to
38 provide to be a gate electrode electrodes of said first
39 MISFET MISFETs over said fourth insulating film portions in
40 said first region, and

41 (i) ~~introducing an impurity on the surface of said~~
42 ~~semiconductor substrate in order to form third~~
43 ~~semiconductor regions having a conductivity type contrary~~
44 ~~to that of said first semiconductor regions on both sides~~
45 ~~of said gate electrode of said first region and a fourth~~
46 ~~semiconductor region having the same conductivity type as~~
47 ~~that of said second semiconductor regions below said first~~
48 ~~opening in said second region~~

49 (i) introducing an impurity on the surface of said
50 semiconductor substrate in order to form second

51 semiconductor regions as portions of the source and drain
52 regions of said first MISFETs in said first region and to
53 form third semiconductor regions as portions of the source
54 and drain regions of said second MISFETs in said second
55 region,
56 wherein each said first semiconductor region is formed
57 deeper than said first insulating film portions in said
58 second region, and
59 wherein each said third semiconductor region is
60 surrounded by a corresponding one of said first
61 semiconductor regions.

Claims 25-26 (cancelled)

1 27. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 24, wherein the first insulating film portions in said
4 first region [[is]] are narrower than the first insulating
5 film portions in said second region.

1 28. (withdrawn) A manufacturing method of a
2 semiconductor integrated circuit device having a first
3 MISFET in a first region of a semiconductor substrate and a

4 second MISFET in a second region, comprising the steps of:

5 (a) forming a first insulating film in said first and
6 second regions,

7 (b) depositing a first conductive film over said first
8 insulating film in said first and second regions,

9 (c) removing the first insulating film and the first
10 conductive film in said first region,

11 (d) forming a second insulating film in said first
12 region over said semiconductor substrate,

13 (e) depositing a second conductive film in said first
14 and second regions, and

15 (f) implanting an impurity to said first and second
16 regions downward from a position above said second
17 conductive film at an energy permitting the impurity to
18 reach the substrate in said first region.

1 29. (withdrawn) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 28, further comprising the steps of:

4 (g) depositing a third conductive film over the second
5 conductive film in each of said first and second regions,
6 and

7 (h) removing a portion of said second and third

8 conductive films in said first region, forming a gate
9 electrode of said first MISFET comprised of the second and
10 third conductive films and removing said second and third
11 conductive films from said second region.

1 30. (withdrawn) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 28, further comprising the steps of:

4 (g) depositing a third conductive film over the second
5 conductive film in each of said first and second regions,

6 (h) removing a portion of said second and third
7 conductive films in said first region, forming a gate
8 electrode of said first MISFET comprised of the second and
9 third conductive films and removing the second and third
10 conductive films from said second region, and

11 (i) removing a portion of said first conductive film
12 from said second region and forming a gate electrode of
13 said second MISFET.

1 31. (withdrawn) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 28, which further comprising the step of:

4 (g) forming a fourth conductive film over said

5 semiconductor substrate within said first region.

1 32. (withdrawn) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 28, wherein implantation of the impurity stops at said
4 first conductive film and the impurity does not reach said
5 first insulating film.

1 33. (withdrawn) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 28, wherein implantation of the impurity stops at said
4 first conductive film and the impurity does not reach said
5 semiconductor substrate in said second region.

1 34. (withdrawn) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 28, wherein said first conductive film is thicker than said
4 second conductive film.

1 35. (withdrawn) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 28, further comprising, between the step (d) and the step
4 (e), heating in a nitrogen-containing atmosphere.

1 36. (withdrawn) A manufacturing method of a
2 semiconductor integrated circuit device having a plurality
3 of first MISFETs in a first region of a semiconductor
4 substrate and a plurality of second MISFETs in a second
5 region, comprising the steps of:

6 (a) forming a first insulating film between two
7 adjacent regions of said first MISFET forming regions in
8 said first region and said second MISFET forming regions in
9 said second regions,

10 (b) forming a second insulating film over a surface of
11 said semiconductor substrate between said first insulating
12 films,

13 (c) depositing a third insulating film over said
14 second insulating film in each of said first and second
15 regions,

16 (d) removing said third insulating film from said
17 first region,

18 (e) forming a first conductive film in said second
19 region,

20 (f) exposing the surface of the semiconductor
21 substrate in said first region while covering said third
22 insulating film in said second region with said first

23 conductive film and forming a fourth insulating film, and
24 (g) forming a second conductive film over the fourth
25 insulating film in said first region.

1 37. (withdrawn) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 36 further having a third region, comprising the steps of:

4 (a) forming the first insulating film in said third
5 region,

6 (b) forming the first conductive film over said first
7 insulating film in said third region,

8 (c) forming a fifth insulating film over said first
9 conductive film in said third region, and

10 (d) forming the second conductive film over the fifth
11 insulating film in said third region.

1 38. (withdrawn) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 37, wherein said first and second conductive films and said
4 fifth insulating film constitute a capacitative element.

1 39. (withdrawn) A manufacturing method of a
2 semiconductor integrated circuit device according to claim
3 36, wherein the first insulating film in said first region
4 is narrower than the first insulating film in said second
5 region.

Claims 40-58 (cancelled)

1 59. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device having a plurality
3 of first MISFETs in a first region of a semiconductor
4 substrate and a plurality of second MISFETs in a second
5 region of said semiconductor substrate, comprising the
6 steps of:

7 (a) forming a plurality of first insulating film
8 portions over a surface of the semiconductor substrate in
9 said first and second regions and a boundary region between
10 said first and second regions,

11 (b) forming a plurality of second insulating film
12 portions between said first insulating film portions over
13 said surface of the semiconductor substrate,

14 ~~[[b]]~~ (c) depositing a second third insulating film
15 over said first and second insulating film portions ~~film in~~
16 ~~said first and second regions,~~

17 (d) patterning said third insulating film in order to
18 retain portions of said third insulating film in said
19 boundary region and said second region,

20 ~~[[c]]~~ (e) forming a first conductive film portion

21 over said second third insulating film portion in said
22 second region,

23 ~~(d) exposing the surface of the semiconductor~~
24 ~~substrate in said first region while covering said second~~
25 ~~insulating film in said second region with said first~~
26 ~~conductive film, and forming a third insulating film, and~~

27 (f) forming a fourth insulating film portion over a
28 surface of said semiconductor substrate in said first
29 region,

30 ~~[[e]]~~ (g) forming a second conductive film portion
31 over the third fourth insulating film portion in said first
32 region,

33 (h) forming a fifth insulating film over said first,
34 second and boundary regions, and

35 (i) forming a plurality of third conductive film
36 portions over said fifth insulating film.

1 60. (Currently amended) A manufacturing method of a
2 semiconductor integrated circuit device having a plurality
3 of first MISFETs in a first region of a semiconductor
4 substrate and a plurality of second MISFETs in a second
5 region of said semiconductor substrate, comprising the
6 steps of:

7 (a) forming a plurality of first insulating film
8 portions made of [[a]] thermally oxidized film on a surface
9 of the semiconductor substrate in said first and second
10 regions and a boundary region between said first and second
11 regions,

12 (b) selectively introducing impurities into said
13 semiconductor substrate, thereby forming first impurity
14 regions in said second region,

15 (c) forming a plurality of second insulating film
16 portions between said first insulating film portions over
17 said surface of the semiconductor substrate,

18 [[(b)]] (d) depositing a second third insulating film
19 over said first and second insulating films film in said
20 first and second regions,

21 (e) patterning said third insulating film in order to
22 retain portions of said third insulating film in said
23 boundary region and said second region,

24 [[(c)]] (f) forming a first conductive film portion
25 over said second third insulating film in said second
26 region,

27 (d) exposing the surface of the semiconductor
28 substrate in said first region while covering said second
29 insulating film in said second region with said first

30 ~~conductive film, and forming a third insulating film made~~
31 ~~of a thermally oxidized film, and~~
32 (g) forming a fourth insulating film portion over a
33 surface of said semiconductor substrate in said first
34 region,
35 [[e)] (h) forming a second conductive film portion
36 over the third fourth insulating film portion in said first
37 region,
38 (i) introducing impurities into said semiconductor
39 substrate, thereby forming second impurity regions,
40 (j) forming a fifth insulating film over said first,
41 second and boundary regions, and
42 (k) forming a third conductive film portion over said
43 fifth insulating film,
44 wherein a portion of said third conductive film
45 portion in said boundary region is formed over a first
46 insulating film portion via portions of said third and
47 fifth insulating films,
48 wherein said first impurity regions and second
49 impurity regions formed in said second region compose
50 source and drain regions of said plurality of second
51 MISFETs,

52 wherein each said first impurity region in said second
53 region surrounds a corresponding second impurity region,
54 and
55 wherein each said first impurity region in said second
56 region surrounds at least one corresponding first
57 insulating film portion.

Please add the following claims:

1 61. (New) A manufacturing method of a semiconductor
2 integrated circuit device having a plurality of MISFETs in
3 a semiconductor substrate, comprising the steps of:
4 (a) forming a plurality of first insulating film
5 portions on a surface of said semiconductor substrate,
6 (b) forming a plurality of second insulating film
7 portions between said first insulating film portions over
8 the surface of said semiconductor substrate,
9 (c) forming a plurality of third insulating film
10 portions over said plurality of first insulating film
11 portions and said second insulating film portions,
12 (d) forming a plurality of first conductive film
13 portions to serve as gate electrodes of said plurality of
14 MISFETs over said third insulating film portions,

15 (e) forming a fourth insulating film in order to cover
16 said plurality of MISFETs, and

17 (f) forming a second conductive film over said fourth
18 insulating film,

19 wherein at least a portion of said second conductive
20 film is formed over a first insulating film portion via a
21 third insulating film portion and a portion of said fourth
22 insulating film.

1 62. (New) A manufacturing method of a semiconductor
2 integrated circuit device having a plurality of MISFETs in
3 a semiconductor substrate, comprising the steps of:

4 (a) forming a plurality of first insulating film
5 portions on a surface of said semiconductor substrate,

6 (b) selectively introducing impurities into said
7 semiconductor substrate, thereby forming first impurity
8 regions,

9 (c) forming a plurality of second insulating film
10 portions between said first insulating film portions over
11 the surface of said semiconductor substrate,

12 (d) forming a plurality third insulating film portions
13 over said first and second insulating film portions,

14 (e) forming a plurality of first conductive film
15 portions to serve as gate electrodes of said plurality of
16 MISFETs over said third insulating film portions, and
17 (f) introducing impurities into said semiconductor
18 substrate, thereby forming second impurity regions,
19 wherein said first impurity regions and second
20 impurity regions compose portions of source and drain
21 regions of said plurality of MISFETs,
22 wherein each said first impurity region surrounds a
23 corresponding second impurity region, and
24 wherein each said first impurity region surrounds at
25 least one corresponding first insulating film portion.

1 63. (New) A manufacturing method of a semiconductor
2 integrated circuit device according to claim 24, wherein
3 the impurity concentration of said first semiconductor
4 regions is lower than that of said third semiconductor
5 regions.

1 64. (New) A manufacturing method of a semiconductor
2 integrated circuit device according to claim 59, wherein
3 said third insulating film is formed by a CVD method.

1 65. (New) A manufacturing method of a semiconductor
2 integrated circuit device according to claim 60, wherein
3 said third insulating film is formed by a CVD method.

1 66. (New) A manufacturing method of a semiconductor
2 integrated circuit device according to claim 60, wherein
3 the impurity concentration of said first impurity regions
4 is lower than that of said second impurity regions.

1 67. (New) A manufacturing method of a semiconductor
2 integrated circuit device according to claim 60, wherein
3 said first insulating film portions formed in said second
4 region are narrower than a first insulating film portion
5 formed in said boundary region.

1 68. (New) A manufacturing method of a semiconductor
2 integrated circuit device according to claim 61, wherein
3 said third insulating film is formed by a CVD method.

1 69. (New) A manufacturing method of a semiconductor
2 integrated circuit device according to claim 62, wherein
3 said third insulating film portions are formed by a CVD
4 method.

1 70. (New) A manufacturing method of a semiconductor
2 integrated circuit device according to claim 62, wherein
3 the impurity concentration of said first impurity regions
4 is lower than that of said second impurity regions.

1 71. (New) A manufacturing method of a semiconductor
2 integrated circuit device according to claim 1, wherein at
3 least one of said plurality of first interconnects is
4 formed over a first insulating film portion via a third
5 insulating film portion and a portion of said fifth
6 insulating film.

1 72. (New) A manufacturing method of a semiconductor
2 integrated circuit device according to claim 13, wherein at
3 least one of said plurality of first interconnects is
4 formed over a first insulating film portion via a third
5 insulating film portion and a portion of said fifth
6 insulating film.

1 73. (New) A manufacturing method of a semiconductor
2 integrated circuit device according to claim 59, wherein at
3 least one of said third conductive film portions is formed

4 over a first insulating film portion via portions of said
5 third and fifth insulating films.